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EVAPORATED $LaAlO_3$ FILMS FOR GATE DIELECTRICS

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Field of the Invention

The invention relates to semiconductor devices and device fabrication. Specifically, the invention relates to gate dielectric layers of transistor devices and their method of fabrication.

Background of the Invention

The semiconductor device industry has a market driven need to improve speed performance, improve its low static (off-state) power requirements, and adapt to a wide range of power supply and output voltage requirements for it silicon based microelectronic products. In particular, in the fabrication of transistors, there is continuous pressure to reduce the size of devices such as transistors. The ultimate goal is to fabricate increasingly smaller and more reliable integrated circuits (ICs) for use in products such as processor chips, mobile telephones, or memory devices such as DRAMs. The smaller devices are frequently powered by batteries, where there is also pressure to reduce the size of the batteries, and to extend the time between battery charges. This forces the industry to not only design smaller transistors, but to design them to operate reliably with lower power supplies.

Currently, the semiconductor industry relies on the ability to reduce or scale the dimensions of its basic devices, primarily, the silicon based metal-oxide-semiconductor field effect transistor (MOSFET). A common configuration of such a transistor is shown in Figure 1. While the following discussion uses Figure 1 to illustrate a transistor from the prior art, one skilled in the art will recognize that the present invention could be incorporated into the transistor shown in Figure 1 to form a novel transistor according to the invention. The transistor 100 is fabricated in a substrate 110 that is typically silicon, but could be fabricated from other semiconductor materials as well. The transistor 100 has a first source/drain region 120 and a second source/drain region 130. A body region

132 is located between the first source/drain region and the second source/drain region, the body region 132 defining a channel of the transistor with a channel length 134. A gate dielectric, or gate oxide 140 is located on the body region 132 with a gate 150 located over the gate dielectric. Although the gate dielectric can be formed from materials other than oxides, the gate dielectric is typically an oxide, and is commonly referred to as a gate oxide. The gate may be fabricated from polycrystalline silicon (polysilicon) or other conducting materials such as metal may be used.

In fabricating transistors to be smaller in size and reliably operating on lower power supplies, one important design criteria is the gate dielectric 140. The mainstay for forming the gate dielectric has been silicon dioxide, SiO_2. Thermally grown amorphous SiO_2 provides a electrically and thermodynamically stable material, where the interface of a SiO_2 layer with an underlying Si provides a high quality interface as well as superior electrical isolation properties. In typical processing, use of SiO_2 on Si has provided defect charge densities on the order of $10^{10}/cm^2$, midgap interface state densities of approximately $10^{10}/cm^2$ eV, and breakdown voltages in the range of 15 MV/cm. With such qualities, there would be no apparent need to use a material other than SiO_2, but with increased scaling, other requirements for gate dielectrics create the need to find other dielectric materials to be used for a gate dielectric.

A gate dielectric 140, when operating in a transistor, has both a physical gate dielectric thickness and an equivalent oxide thickness (t_{eq}). The equivalent oxide thickness quantifies the electrical properties, such as capacitance, of a gate dielectric 140 in terms of a representative physical thickness. t_{eq} is defined as the thickness of a theoretical SiO_2 layer that would be required to have the same capacitance density as a given dielectric, ignoring leakage current and reliability considerations. A SiO_2 layer of thickness, t, deposited on a Si surface as a gate dielectric will also have a t_{eq} larger than its thickness, t. This t_{eq} results from the capacitance in the surface channel on which the SiO_2 is deposited due to the formation of a depletion/inversion region. This depletion/inversion region can result in t_{eq} being from 3 to 6 Angstroms (Å) larger than the SiO_2 thickness, t. Thus, with the semiconductor industry driving to someday scale the

gate dielectric equivalent oxide thickness, t_{eq}, to under 10 Å, the physical thickness requirement for a SiO_2 layer used for a gate dielectric would be need to be approximately 4 to 7 Å. Additional requirements on a SiO_2 layer would depend on the gate electrode used in conjunction with the SiO_2 gate dielectric. Using a conventional polysilicon gate would result in an additional increase in t_{eq} for the SiO_2 layer. This additional thickness could be eliminated by using a metal gate electrode, though metal gates are not currently used in complementary metal-oxide-semiconductor field effect transistor (CMOS) technology. Thus, future devices would be designed towards a physical SiO_2 gate dielectric layer of about 5 Å or less. Such a small thickness requirement for a SiO_2 oxide layer creates additional problems.

Silicon dioxide is used as a gate dielectric, in part, due to its electrical isolation properties in a SiO_2 - Si based structure. This electrical isolation is due to the relatively large band gap of SiO_2 (8.9 eV) making it a good insulator from electrical conduction. Signification reductions in its band gap would eliminate it as a material for a gate dielectric. As the thickness of a SiO_2 layer decreases, the number of atomic layers, or monolayers of the material in the thickness decreases. At a certain thickness, the number of monolayers will be sufficiently small that the SiO_2 layer will not have a complete arrangement of atoms as in a larger or bulk layer. As a result of incomplete formation relative to a bulk structure, a thin SiO_2 layer of only one or two monolayers will not form a full band gap. The lack of a full band gap in a SiO_2 gate dielectric would cause an effective short between an underlying Si channel and an overlying polysilicon gate. This undesirable property sets a limit on the physical thickness to which a SiO_2 layer can be scaled. The minimum thickness due to this monolayer effect is thought to be about 7-8 Å. Therefore, for future devices to have a t_{eq} less than about 10 Å, other dielectrics than SiO_2 need to be considered for use as a gate dielectric.

For a typical dielectric layer used as a gate dielectric, the capacitance is determined as one for a parallel plate capacitance: $C = \kappa\epsilon_0 A/t$, where κ is the dielectric constant, ϵ_0 is the permittivity of free space, A is the area of the capacitor, and t is the

thickness of the dielectric. The thickness, t, of a material is related to t_{eq} for a given capacitance with the dielectric constant of SiO_2, $\kappa_{ox} = 3.9$, associated with t_{eq}, as

$$t = (\kappa/\kappa_{ox}) t_{eq} = (\kappa/3.9) t_{eq}.$$

Thus, materials with a dielectric constant greater than that of SiO_2, 3.9, will have a physical thickness that can be considerably larger than a desired t_{eq}, while providing the desired equivalent oxide thickness. For example, an alternate dielectric material with a dielectric constant of 10 could have a thickness of about 25.6 Å to provide a t_{eq} of 10 Å, not including any depletion/inversion layer effects. Thus, the reduced equivalent oxide thickness of transistors can be realized by using dielectric materials with higher dielectric constants than SiO_2.

The thinner equivalent oxide thickness, $t_{eq,}$ required for lower transistor operating voltages and smaller transistor dimensions may be realized by a significant number of materials, but additional fabricating requirements makes determining a suitable replacement for SiO_2 difficult. The current view for the microelectronics industry is still for Si based devices. This requires that the gate dielectric employed be grown on a silicon substrate or silicon layer, which places significant restraints on the substitute dielectric material. During the formation of the dielectric on the silicon layer, there exists the possibility that a small layer of SiO_2 could be formed in addition to the desired dielectric. The result would effectively be a dielectric layer consisting of two sublayers in parallel with each other and the silicon layer on which the dielectric is formed. In such a case, the resulting capacitance would be that of two dielectrics in series. As a result, the t_{eq} of the dielectric layer would be the sum of the SiO_2 thickness and a multiplicative factor of the thickness of the dielectric being formed. Thus, if a SiO_2 layer is formed in the process, the t_{eq} is again limited by a SiO_2 layer. In the event, that a barrier layer is formed between the silicon layer and the desired dielectric in which the barrier layer prevents the formation of a SiO_2 layer, the t_{eq} would be limited by the layer with the lowest dielectric constant. However, whether a single dielectric layer with a high dielectric constant or a barrier layer with a higher dielectric constant than SiO_2 is

employed, the layer interfacing with the silicon layer must provide a high quality interface to maintain a high channel carrier mobility.

What is needed is an alternate dielectric material for forming a gate dielectric that has a high dielectric constant relative to SiO_2, and is thermodynamically stable with respect to silicon such that forming the dielectric on a silicon layer will not result in SiO_2 formation, or diffusion of material, such as dopants, into the gate dielectric from the underlying silicon layer.

Summary of the Invention

A solution to the problems as discussed above is addressed in the present invention. In accordance with the present invention, a method of forming a gate dielectric on a transistor body region includes evaporating Al_2O_3 at a given rate, evaporating La_2O_3 at another rate, and controlling the first rate and the second rate to provide an amorphous film containing $LaAlO_3$ on the transistor body region. The evaporation deposition of the $LaAlO_3$ film is performed using two electron guns to evaporate dry pellets of Al_2O_3 and La_2O_3. The two rates for evaporating the materials are selectively chosen to provide a dielectric film composition having a predetermined dielectric constant ranging from the dielectric constant of an Al_2O_3 film to the dielectric constant of a La_2O_3 film.

A transistor is fabricated by forming two source/drain regions separated by a body region, evaporating Al_2O_3 using an electron gun at one rate, evaporating La_2O_3 using a second electron gun at a second rate, controlling the two evaporation rates to provide a film containing $LaAlO_3$ on the body region, and forming a conductive gate on the film containing $LaAlO_3$. Dry pellets of Al_2O_3 and La_2O_3 are used for evaporating Al_2O_3 and La_2O_3. Controlling the two rates provides the capability to form a film composition having a predetermined dielectric constant.

Advantageously, these methods can be used to further form a memory array where the process of forming the memory is adapted to form the gate dielectric in accordance with the present invention. Additionally, an information handling system can be formed

using the methods of the present invention, wherein a memory array formed in conjunction with forming a processor is formed to include transistors having gate dielectrics containing $LaAlO_3$. These gate dielectrics are formed by evaporating Al_2O_3 using an electron gun at one rate, evaporating La_2O_3 using a second electron gun at a second rate, and controlling the two evaporation rates to provide a film containing $LaAlO_3$ for use as the gate dielectric.

In accordance with the present invention, a transistor having two source/drain regions separated by a body region includes an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions. The gate dielectric may be essentially composed of $LaAlO_3$ or it may also contain Al_2O_3, and La_2O_3. Depending on its composition, the dielectric constant of the gate dielectric can range from about 9 to about 30. Depending on its composition, the gate dielectric can have a thickness corresponding to an equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms, in addition to larger t_{eq} values.

Advantageously, a memory array includes a number of transistors having two source/drain regions separated by a body region with an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions. These transistors provide the memory array with an array of transistors having gate dielectrics with equivalent oxide thickness (t_{eq}) in the range from about 1.5 Angstroms to about 5 Angstroms, providing transistors operable at reduced voltage levels. Additionally, an information handling device, such as a computer, includes a processor and a memory array having a number of transistors having two source/drain regions separated by a body region that includes an amorphous gate dielectric containing $LaAlO_3$ located above the body region between the two source/drain regions.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the

invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1 depicts a common configuration of a transistor.

Figure 2 depicts a deposition process in accordance with the present invention.

Figure 3 depicts another configuration of a transistor capable of being fabricated in accordance with the present invention.

Figure 4 depicts a perspective view of a personal computer incorporating devices made in accordance with the present invention.

Figure 5 depicts a schematic view of a central processing unit incorporating devices made in accordance with the present invention.

Figure 6 shows a schematic view of a DRAM memory device in accordance with the present invention.

Detailed Description of the Preferred Embodiments

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator or dielectric is defined to include any material that is less electrically conductive than the materials referred to as conductors.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

In a recent article by G. D. Wilk et al., Journal of Applied Physics, vol. 89: no. 10, pp. 5243-5275 (2001), material properties of high dielectric materials for gate dielectrics were discussed. Among the information disclosed was the viability of Al_2O_3 as a substitute for SiO_2. Al_2O_3 was disclosed has having favourable properties for use as a gate dielectric such as high band gap, thermodynamic stability on Si up to high temperatures, and an amorphous structure. In addition, Wilk disclosed that forming a layer of Al_2O_3 on silicon does not result in a SiO_2 interfacial layer. However, the dielectric constant of Al_2O_3 is only 9, where thin layers may have a dielectric constant of about 8 to about 10. Though the dielectric constant of Al_2O_3 is in an improvement over

SiO_2, a higher dielectric constant for a gate dielectric is desirable. Other dielectrics and their properties discussed by Wilk include

Material	Dielectric Constant (κ)	Band gap E_g (eV)	Crystal Structure(s)
SiO_2	3.9	8.9	Amorphous
Si_3N_4	7	5.1	Amorphous
Al_2O_3	9	8.7	Amorphous
Y_2O_3	15	5.6	Cubic
La_2O_3	30	4.3	Hexagonal, Cubic
Ta_2O_3	26	4.5	Orthorhombic
TiO_2	80	3.5	Tetrag. (rutile, anatase)
HfO_2	25	5.7	Mono., Tetrag., Cubic
ZrO_2	25	7.8	Mono., Tetrag., Cubic

One of the advantages using SiO_2 as a gate dielectric has been that the formation of the SiO_2 layer results is an amorphous gate dielectric. Having an amorphous structure for a gate dielectric is advantageous because grain boundaries in polycrystalline gate dielectrics provide high leakage paths. Additionally, grain size and orientation changes throughout a polycrystalline gate dielectric can cause variations in the film's dielectric constant. The abovementioned material properties including structure are for the materials in a bulk form. The materials having the advantage of a high dielectric constants relative to SiO_2 also have the disadvantage of a crystalline form, at least in a bulk configuration. The best candidates for replacing SiO_2 as a gate dielectric are those with high dielectric constant, which can be fabricated as a thin layer with an amorphous form.

Reportedly, a physical thickness of about 21 Å of Al_2O_3, grown by thermal oxidation following thermal evaporation of an Al layer, could be obtained providing a t_{eq} of 9.6 Å with an interface state density greater than or equal to $3x10^{10}$ eV^{-1} cm^{-2}. Higher physical thicknesses of about 48 Å of Al_2O_3 provided films with t_{eq} of 21 Å with leakage

current of approximately 10^{-8} A/cm^2 at 1 V gate bias, which is good when compared to a leakage current of 10^{-1} A/cm^2 at 1 V gate bias for a physical thickness of 21 Å for a pure SiO_2 layer.

Another abovementioned material, La_2O_3, reportedly provided good results when fabricating thin films on silicon. A physical thickness of 33 Å was obtained for a layer of La_2O_3, grown by thermal oxidation following thermal evaporation of a La layer, providing a t_{eq} of 4.8 Å, a leakage current of 10^{-1} A/cm^2 at 1 V gate bias, and an interface state density of approximately $3x10^{10}$ eV^{-1} cm^{-2}. Other studies on La_2O_3 showed reduced leakage current but an interfacial SiO_x layer.

Though both Al_2O_3 and La_2O_3 demonstrated good qualities as a substitute for SiO_2, better dielectrics are needed. In a recent article by B. Park et al., Applied Physics Letters, vol. 79: no. 6, pp. 806- 808 (2001), use of $LaAlO_3$ on silicon as a buffer layer between the silicon surface and a ferroelectric film was reported. A $LaAlO_3$ film was deposited on a silicon substrate by heating single crystal pellets of $LaAlO_3$ using an electron gun with the substrate maintained at room temperature. The $LaAlO_3$ film was annealed ex situ in an electric furnace at 700°C for 10 minutes in N_2 ambience. Films having thickness from 18 nm to 80 nm were grown. The resultant films were determined to have a leakage current density decreased by about three orders of magnitude after annealing. This reported experimentation providing a $LaAlO_3$ buffer layer between silicon and a ferroelectric film demonstrated that a $LaAlO_3$ film could be obtained on silicon providing an amorphous dielectric layer with a dielectric constant between 21 and 24. Other reports indicate that $LaAlO_3$ film can be grown by metal-organic chemical-vapor-deposition method, pulsed-laser depositions method, and rf magnetron sputtering method.

In accordance with the present invention, layers of $LaAlO_3$ can be deposited on silicon using low cost starting materials and resulting in dielectric layers whose dielectric constant can be chosen to range from the dielectric constant of Al_2O_3 to the dielectric constant of La_2O_3. Advantageously, a layer of $LaAlO_3$ is grown using dry pellets of Al_2O_3 and La_2O_3. The gate dielectric is formed on a silicon substrate or silicon layer by

electron beam evaporation of the dry pellets of using two electron guns controlled by two rate monitors. Controlling the rates for evaporating the dry pellets Al_2O_3 and La_2O_3 allows for the formation of a gate dielectric having a composition with a predetermined dielectric constant. The predetermined dielectric constant will range from the dielectric constant of Al_2O_3 to the dielectric constant of La_2O_3, depending on the composition of the film. The composition of the film can be shifted more towards an Al_2O_3 film or more towards a La_2O_3 film, depending upon the choice of the dielectric constant.

Figure 2 depicts an electron beam evaporation technique to deposit a material forming a film containing $LaAlO_3$ on a surface such as a body region of a transistor. In Figure 2, a substrate 210 is placed inside a deposition chamber 260. The substrate in this embodiment is masked by a first masking structure 270 and a second masking structure 271. In this embodiment, the unmasked region 233 includes a body region of a transistor, however one skilled in the art will recognize that other semiconductor device structures may utilize this process. Also located within the deposition chamber 260 is an electron gun 263, a second electron gun 265, a target 261, and a second target 262. The first electron gun 263 provides an electron beam 264 directed at target 261 containing dry pellets of Al_2O_3. The second electron gun 265 provides an electron beam 266 directed at target 262 containing dry pellets of La_2O_3. The electron guns individually include a rate monitor for controlling the rate of evaporation of the material in the target at which each individual beam is directed. Evaporating the dry pellets of Al_2O_3 and La_2O_3 is individually controlled using the rate monitors of electron gun 263 and electron gun 265 to form a layer 240 having a composition containing $LaAlO_3$ having a predetermined dielectric constant. For convenience, control displays and necessary electrical connections as are known to those skilled in the art are not shown in Figure 2.

Alternatively, one target containing dry pellets of Al_2O_3 and La_2O_3 could be used with one electron gun. However, in such an arrangement, the individual evaporation of Al_2O_3 and La_2O_3 could not be controlled, not allowing for forming a film composition with a

predetermined dielectric constant. Although in one embodiment, an electron beam evaporation technique is used, it will be apparent to one skilled in the art that other thermal evaporation techniques can be used without departing from the scope of the invention.

During the evaporation process, the electron guns 263, 265 generate electron beams 264, 266. Beginning the evaporation process using electron gun 265 is performed substantially concurrent with beginning the evaporation process using electron gun 265. The electron beam 264 hits target 261 containing dry pellets of Al_2O_3, and heats a portion of target 261 enough to cause the dry pellets of Al_2O_3 on the surface of the target 261 to evaporate. The evaporated material 268 is then distributed throughout the chamber 260. The electron beam 266 hits target 262 containing dry pellets of La_2O_3, and heats a portion of target 262 enough to cause the dry pellets of La_2O_3 the surface of the target 262 to evaporate. The evaporated material 269 is then distributed throughout the chamber 260. Evaporate material 268 and evaporate material 269 are intermingled throughout the chamber forming a film 240 containing $LaAlO_3$ on the surface of the exposed body region 233 that it contacts.

The evaporation process can be performed in chamber 260 using a base pressure lower than about $5x10^{-7}$ Torr and a deposition pressure less than about $2x10^{-6}$ Torr. Performing the evaporation under these conditions should allow a growth rate in the range from about 0.5 to about 50 nm/min. After deposition, the wafer or substrate 210 containing the film is annealed ex situ in an electric furnace at about 700°C for about 10 minutes in N_2 ambience. Alternately, the wafer or substrate 210 can be annealed by RTA for about 10 to about 15 seconds in N_2 ambience.

The $LaAlO_3$ dielectric film should have a dielectric constant in the range of about 21 to about 25. However, by controlling the evaporation rates of the first electron gun 263 and the second electron gun 265, the composition of the film can vary from be a film of essentially Al_2O_3 to a film that is essentially La_2O_3. Correspondingly, the dielectric constant of the formed film will range from about 9 to about 30, with a dielectric constant in the range of about 21 to about 25 corresponding to a layer that is essentially $LaAlO_3$.

Thus, choosing a predetermined dielectric constant in the range of about 9 to about 30, the two electron guns will be controlled to formed a film containing Al_2O_3, La_2O_3, and $LaAlO_3$ in varying amounts depending on the setting for controlling the evaporation rates.

A range of equivalent oxide thickness, t_{eq}, attainable in accordance with the present invention is associated with the capability to provide a composition having a dielectric constant in the range form about 9 to about 30, and the capability to attain growth rates in the range of from about 0.5 to about 50 nm/min . The t_{eq} range in accordance with the present invention are shown in the following

	Physical Thickness t = 0.5 nm (5 Å)	Physical Thickness t = 1.0 nm (10 Å)	Physical Thickness t = 50 nm (500 Å)
κ	t_{eq} (Å)	t_{eq} (Å)	t_{eq} (Å)
9	2.17	4.33	216.67
21	.93	1.86	92.86
25	.78	1.56	78
30	.65	1.3	65

$LaAlO_3$ in a bulk form at room temperature has a nearly cubic perovskite crystal structure with a lattice constant of 0.536 nm. Fortunately, the films grown by electron gun evaporation have an amorphous form, though it is expected that a dimension for a monolayer of $LaAlO_3$ is related to its lattice constant in bulk form. At a physical thickness about .5 nm, t_{eq} would be expected to range from about 2.2 Å to about 0.65 Å for the dielectric constant ranging from 9 to 30. For a layer of essentially $LaAlO_3$, t_{eq} would be expected to range from about 0.93 Å to about 0.78 Å for a physical layer of 0.5 nm. The lower limit on the scaling of a layer containing $LaAlO_3$ would depend on the monolayers of the film necessary to develop a full band gap such that good insulation is maintained between an underlying silicon layer and an overlying conductive layer to the $LaAlO_3$ film. This requirement is necessary to avoid possible short circuit effects between the underlying silicon layer and the overlying conductive layer. For a substantially $LaAlO_3$ film having a thickness of approximately 2 nm, t_{eq} would range

from about 3 Å to about 3.7 Å. From above, it is apparent that a film containing $LaAlO_3$ can be attained with a t_{eq} ranging from 1.5 Å to 5 Å . Further, such a film can provide a t_{eq} significantly less than 2 or 3 Å, even less than 1.5 Å.

The novel process described above provides significant advantages by evaporating dry pellets of Al_2O_3 and La_2O_3. Dry pellets of Al_2O_3 and La_2O_3 are less expensive than single crystal pellets of $LaAlO_3$. Further, using two electron guns allows the formation of a gate dielectric with a chosen dielectric constant. Additionally, the novel process can be implemented to form transistors, memory devices, and information handling devices.

A transistor 100 as depicted in Figure 1 can be formed by forming a source/drain region 120 and another source/drain region 130 in a silicon based substrate 110 where the two source/drain regions 120, 130 are separated by a body region 132. The body region 132 separated by the source/drain 120 and the source/drain 130 defines a channel having a channel length 134. Al_2O_3 is evaporated using an electron gun at a controlled rate. La_2O_3 is evaporated using a second electron gun at a second controlled rate. Evaporating the Al_2O_3 source is begun substantially concurrent with evaporating La_2O_3, forming a film 140 containing $LaAlO_3$ on the body region. A gate is formed over the gate dielectric 140. Typically, forming the gate includes forming a polysilicon layer, though a metal gate can be formed in an alternative process. Forming the substrate, source/region regions, and the gate is performed using standard processes known to those skilled in the art. Additionally, the sequencing of the various elements of the process for forming a transistor is conducted with standard fabrication processes, also as known to those skilled in the art.

The method of evaporating $LaAlO_3$ films for a gate dielectric in accordance with the present invention can be applied to other transistor structures having dielectric layers. For example, the structure of Figure 3 depicts a transistor 300 having a silicon based substrate 310 with two source/drain regions 320, 330 separated by a body region 332. The body region 332 between the two source/drain regions 320, 330 defines a channel region having a channel length 334. Located above the body region 332 is a stack 355

including a gate dielectric 340, a floating gate 352, a floating gate dielectric 342, and control gate 350. The gate dielectric 340 can be formed as described above with the remaining elements of the transistor 300 formed using processes known to those skilled in the art. Alternately, both the gate dielectric 340 and the floating gate dielectric 342 can be formed in accordance with the present invention as described above.

Transistors created by the methods described above may be implemented into memory devices and information handling devices as shown in Figures 5-7 and described below. While specific types of memory devices and computing devices are shown below, it will be recognized by one skilled in the art that several types of memory devices and information handling devices could utilize the invention.

A personal computer, as shown in Figures 4 and 5, include a monitor 400, keyboard input 402 and a central processing unit 404. The processor unit typically includes microprocessor 506, memory bus circuit 508 having a plurality of memory slots 512(a-n), and other peripheral circuitry 510. Peripheral circuitry 510 permits various peripheral devices 524 to interface processor-memory bus 520 over input/output (I/O) bus 522. The personal computer shown in Figures 4 and 5 also includes at least one transistor having a gate dielectric according to the teachings of the present invention.

Microprocessor 506 produces control and address signals to control the exchange of data between memory bus circuit 508 and microprocessor 506 and between memory bus circuit 508 and peripheral circuitry 510. This exchange of data is accomplished over high speed memory bus 520 and over high speed I/O bus 522.

Coupled to memory bus 520 are a plurality of memory slots 512(a-n) which receive memory devices well known to those skilled in the art. For example, single in-line memory modules (SIMMs) and dual in-line memory modules (DIMMs) may be used in the implementation of the present invention.

These memory devices can be produced in a variety of designs which provide different methods of reading from and writing to the dynamic memory cells of memory slots 512. One such method is the page mode operation. Page mode operations in a DRAM are defined by the method of accessing a row of a memory cell arrays and

randomly accessing different columns of the array. Data stored at the row and column intersection can be read and output while that column is accessed. Page mode DRAMs require access steps which limit the communication speed of memory circuit 508. A typical communication speed for a DRAM device using page mode is approximately 33 MHZ.

An alternate type of device is the extended data output (EDO) memory which allows data stored at a memory array address to be available as output after the addressed column has been closed. This memory can increase some communication speeds by allowing shorter access signals without reducing the time in which memory output data is available on memory bus 520. Other alternative types of devices include SDRAM, DDR SDRAM, SLDRAM and Direct RDRAM as well as others such as SRAM or Flash memories.

Figure 6 is a block diagram of an illustrative DRAM device 600 compatible with memory slots 512(a-n). The description of DRAM 600 has been simplified for purposes of illustrating a DRAM memory device and is not intended to be a complete description of all the features of a DRAM. Those skilled in the art will recognize that a wide variety of memory devices may be used in the implementation of the present invention. The example of a DRAM memory device shown in Figure 6 includes at least one transistor having a gate dielectric according to the teachings of the present invention.

Control, address and data information provided over memory bus 520 is further represented by individual inputs to DRAM 600, as shown in Figure 6. These individual representations are illustrated by data lines 602, address lines 604 and various discrete lines directed to control logic 606.

As is well known in the art, DRAM 600 includes memory array 610 which in turn comprises rows and columns of addressable memory cells. Each memory cell in a row is coupled to a common wordline. The wordline is coupled to gates of individual transistors, where at least one transistor has a gate coupled to a gate dielectric containing

$LaAlO_3$ in accordance with the method and structure previously described above. Additionally, each memory cell in a column is coupled to a common bitline. Each cell in memory array 610 includes a storage capacitor and an access transistor as is conventional in the art.

DRAM 600 interfaces with, for example, microprocessor 606 through address lines 604 and data lines 602. Alternatively, DRAM 600 may interface with a DRAM controller, a micro-controller, a chip set or other electronic system. Microprocessor 506 also provides a number of control signals to DRAM 600, including but not limited to, row and column address strobe signals RAS and CAS, write enable signal WE, an output enable signal OE and other conventional control signals.

Row address buffer 612 and row decoder 614 receive and decode row addresses from row address signals provided on address lines 604 by microprocessor 506. Each unique row address corresponds to a row of cells in memory array 610. Row decoder 614 includes a wordline driver, an address decoder tree, and circuitry which translates a given row address received from row address buffers 612 and selectively activates the appropriate wordline of memory array 610 via the wordline drivers.

Column address buffer 616 and column decoder 618 receive and decode column address signals provided on address lines 604. Column decoder 618 also determines when a column is defective and the address of a replacement column. Column decoder 618 is coupled to sense amplifiers 620. Sense amplifiers 620 are coupled to complementary pairs of bitlines of memory array 610.

Sense amplifiers 620 are coupled to data-in buffer 622 and data-out buffer 624. Data-in buffers 622 and data-out buffers 624 are coupled to data lines 602. During a write operation, data lines 602 provide data to data-in buffer 622. Sense amplifier 620 receives data from data-in buffer 622 and stores the data in memory array 610 as a charge on a capacitor of a cell at an address specified on address lines 604.

During a read operation, DRAM 600 transfers data to microprocessor 506 from memory array 610. Complementary bitlines for the accessed cell are equilibrated during a precharge operation to a reference voltage provided by an equilibration circuit and a

reference voltage supply. The charge stored in the accessed cell is then shared with the associated bitlines. A sense amplifier of sense amplifiers 620 detects and amplifies a difference in voltage between the complementary bitlines. The sense amplifier passes the amplified voltage to data-out buffer 624.

Control logic 606 is used to control the many available functions of DRAM 600. In addition, various control circuits and signals not detailed herein initiate and synchronize DRAM 600 operation as known to those skilled in the art. As stated above, the description of DRAM 600 has been simplified for purposes of illustrating the present invention and is not intended to be a complete description of all the features of a DRAM. Those skilled in the art will recognize that a wide variety of memory devices, including but not limited to, SDRAMs, SLDRAMs, RDRAMs and other DRAMs and SRAMs, VRAMs and EEPROMs, may be used in the implementation of the present invention. The DRAM implementation described herein is illustrative only and not intended to be exclusive or limiting.

Conclusion

A gate dielectric containing $LaAlO_3$ and method of fabricating a gate dielectric contained $LaAlO_3$ are provided that produces a reliable gate dielectric having a thinner equivalent oxide thickness than attainable using SiO_2. $LaAlO_3$ gate dielectrics formed using the methods described herein are thermodynamically stable such that the gate dielectrics formed will have minimal reactions with a silicon substrate or other structures during processing.

Transistors and higher level ICs or devices are provided utilizing the novel gate dielectric and process of formation. Gate dielectric layers containing $LaAlO_3$ are formed having a high dielectric constant (κ) capable of a t_{eq} thinner than 5 Å, thinner than the expected limit for SiO_2 gate dielectrics. At the same time, the physical thickness of the $LaAlO_3$ layer is much larger than the SiO_2 thickness associated with the t_{eq} limit of SiO_2.

Forming the larger thickness provides advantages in processing the gate dielectric. In addition forming a dielectric containing $LaAlO_3$, Al_2O_3, and La_2O_3 through controlling the evaporation of Al_2O_3 and La_2O_3 sources allows the selection of a dielectric constant ranging from that of Al_2O_3 to the dielectric constant of La_2O_3.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.